Joint Online Faculty Development Programme

RISC-V VLSI Implementation Flow: RTL2GDS

Feb 7 – Feb 12, 2022

Organized by

IIT Guwahati, MNIT Jaipur, NIT Patna & PDPM IIITDM Jabalpur

Course Contents

- Transistor to Processor Level Simulation and Verification
- Digital Blocks constituting RISCV Processor
- Digital Design to Processor ISA
- RISCV Instruction Set Architecture
- ISA Simulators
- Simulation and Verification of RISCV ISA
- RISCV Processor Design from Ground Up
- Visualization of Processor blocks via Synthesis
- Overview of RTL2GDS flow in processor design
- Tapeout SignOff for Processor: What does it mean?
- Power Performance Area Tradeoffs in RISCV Processor Design
- RISC V Job Market

Speakers

- Prof. M. Balakrishnan,
- Prof. Anshul Kumar, IIT Delhi,
- Prof. Preeti Ranjan Panda, IIT Delhi;
- Prof. V. Kamakoti, IITM (consent awaited); Mr. Gaurav Jalan, Founder SpicaWorks, Bengaluru

Joint Principal Coordinator

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Programme Features

- Instructor led online sessions and rigorous hands-on sessions.
- Opportunities to connect with experts from academia, industry and government
- Certificate of completion on successful completion of the course with full access to the course material.

Registration Details

Registration link –
https://forms.gle/g8VHYBHmnFybbrdK9

Registration fee

Indian Participants –
Academic (student/faculty): 500 INR
Industry Participants and Others : 1000 INR

Foreign Participants –
SAARC/African countries
Academic (student/faculty): - Rs. 500/-
Others - Rs. 1000/-

Rest of the countries
Fee - US$ 60 or British £ 50

Last Date for Registration : Feb 5, 2022

Online payment details
Beneficiary Name : EICT Academy
Bank Name: INDIAN BANK
A/C No. : 50302042708
IFSC Code: IDIB000M694
Branch: Mehgawan, IIITDM Branch

Contact Us

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